AN938
APPLICATION NOTE

DESIGNING WITH L4973, 3.5A HIGH EFFICIENCY DC-DC CONVERTER

1 INTRODUCTION

The L4973 family is a 3.5A monolithic dc-dc converter, step- down topology, operating in continuous mode. It is realized in BCD60 II technology, and it's available in two plastic packages, POWERDIP18(12+3+3) and SO20L (12+4+4).

Two versions are available, one fixing the output voltage, without any voltage divider, at 3.3V, and the second at 5.1V.

Both the regulators can control higher output voltage values, by using an external voltage divider.

The operating input supply voltage is ranging from 8V to 55V, while the absolute value, with no load, is 60V.

New internal design solutions and superior technology performance allowed us to develop and produce a device with improved efficiency in all the operating conditions and reduced external component counts.

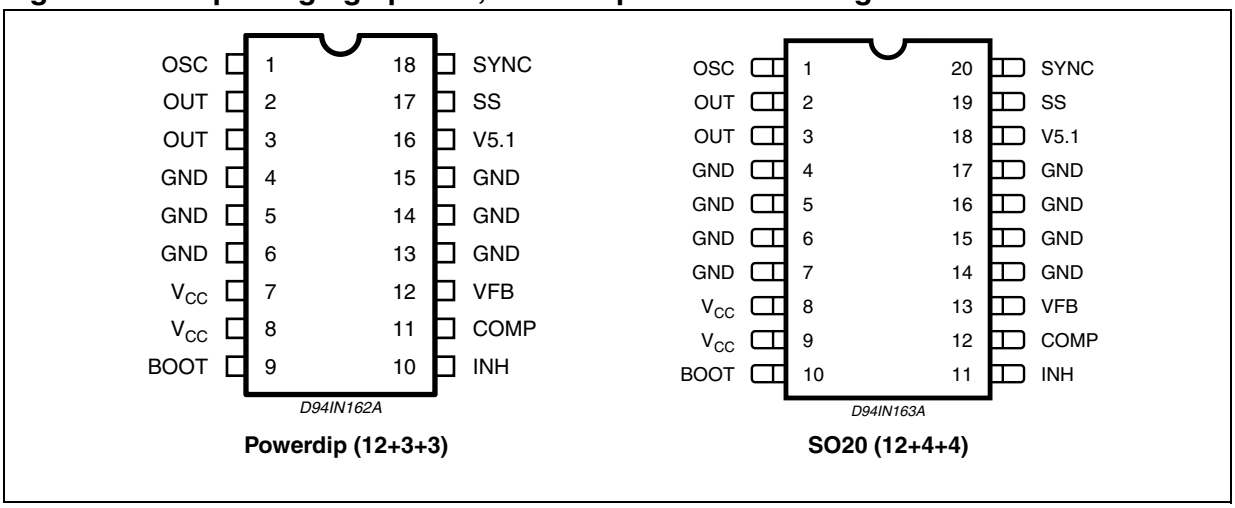
While internal limiting current and thermal shutdown are today considered standard protections functions mandatory for a safe load supply, oscillator with voltage feedforward will improve line regulation and overall control loop. Soft-start does not allow output overvoltages at turn-on, and synchronization function can reduce EMI problems in multioutputs power supplies. Inhibit, introduced for power management, in equipments having stand-by features, when active(high), reduces the device power consumption, signal plus power stages, at few tens of μA.

Figure 1.

2 DEVICE DESCRIPTION

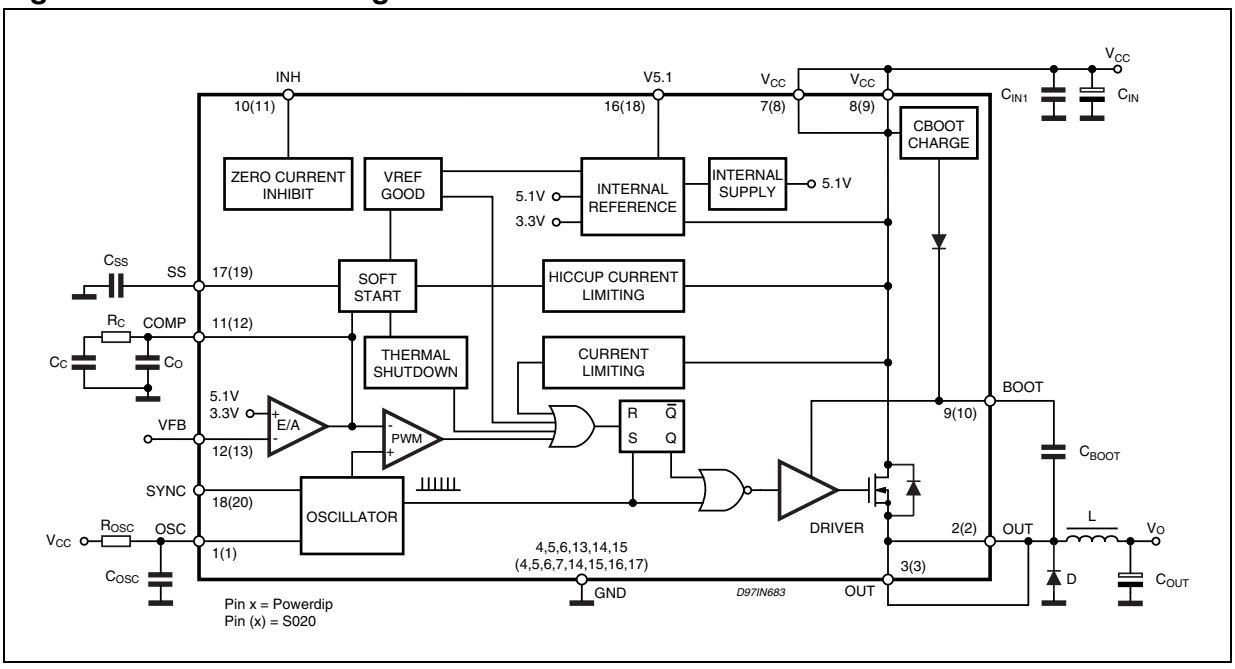
For a better understanding of the device and it's working principle, a short description of the main building blocks is given here below, with packaging options and complete block diagram.

Figure 2. Two packaging options, with the pin function assignements.



Powerdip (12+3+3) **SO20 (12+4+4)**

Figure 3. Device block diagram.



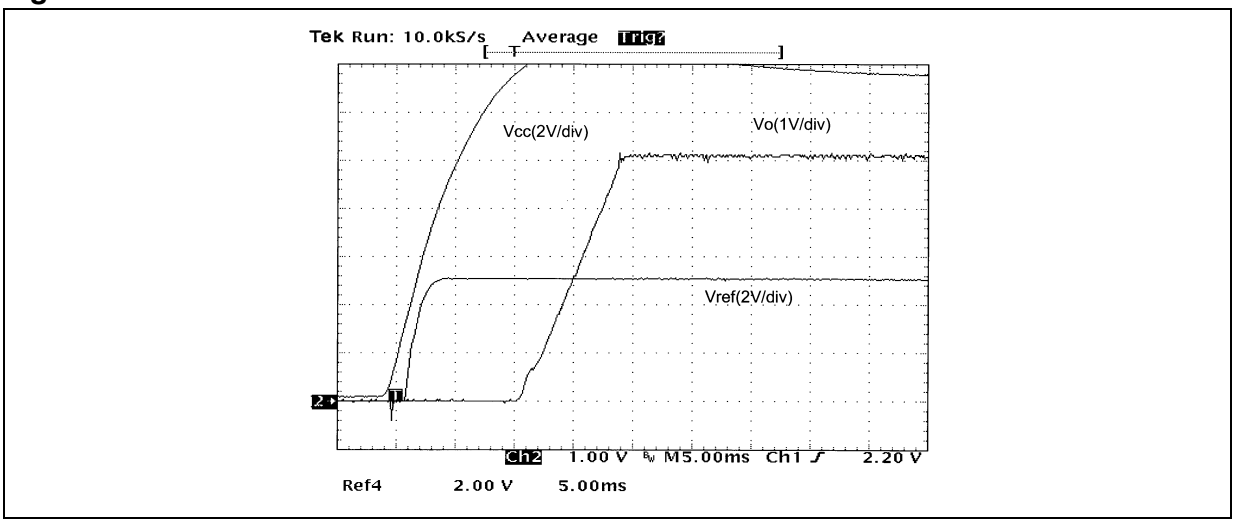
3 POWER SUPPLY, UVLO AND VOLTAGE REFERENCE.

The device is provided with an internal stabilised power supply (of about 12V typ.) that powers the analog and digital control blocks and the bootstrap section.

Moreover, a safe turn-on sequence is guaranteed by an internal UVLO.

When the supply voltage is reaching about 3.8V, the band-gap goes into regulation, while the internal 5.1V reference starts to increase from zero to its nominal value.

Figure 4.



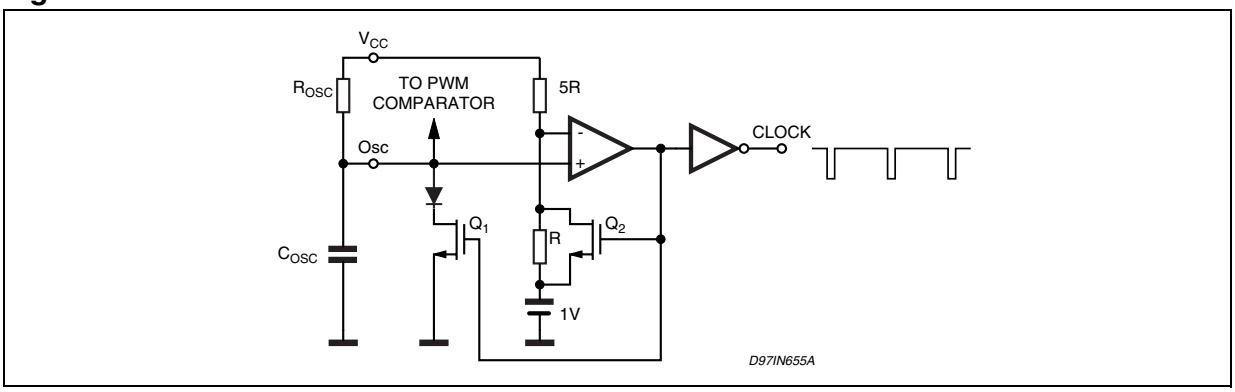
At 6.5V of Vcc, the device initiates to charge the soft-start capacitor and the power stage generates the first pwm pulses.

The output voltage increases with a slope controlled by the soft-start rime. Fig. 4 shows the turn-on sequence of the mentioned signals.

From the 12V preregulator, a stable 5.1V ±2% reference voltage, externally available, is generated, with a 10mA of current capability.

This reference is available on both types, while the feedback reference is 5.1V for the L4973V5.1 and 3.3V for the L4973V3.3.

Figure 5. Oscillator Internal Circuit



3.1 Oscillator, sync and voltage feedforward

One pin is necessary to implement the oscillator function, with inherent voltage feedforward; a second pin is dedicated to in/out synchronization.

A resistor Rosc and a capacitor Cosc connected as shown in fig. 5, allow the setting of the desired switching frequency in agreement with the below formula:

$$F_{SW} = \frac{1}{(R_{oasc} \cdot C_{osc}) \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

Where Fsw is in kHz, Rosc in KΩ and Cosc in nF.

The oscillator capacitor, Cosc, is discharged by an internal mos transistor of 100Ω of Rdson (Q1) and during this period the internal threshold is setted at 1V by a second mos, Q2 . When the oscillator voltage capacitor reaches the 1V threshold the output comparator turn-off the mos Q1 and turn-on the mos Q2, restarting the Cosc charging. The oscillator block, shown in fig. 5, generates a sawtooth wave signal that sets the switching frequency of the system.
This signal, compared with the output of the error amplifier, generates the PWM signal that will modulate the conduction time of the power output stage.
The way the oscillator has been integrated,does not require additional external components to benefit of the voltage feedforward function.

Figure 6. Device switching frequency vs Rosc and Cosc.

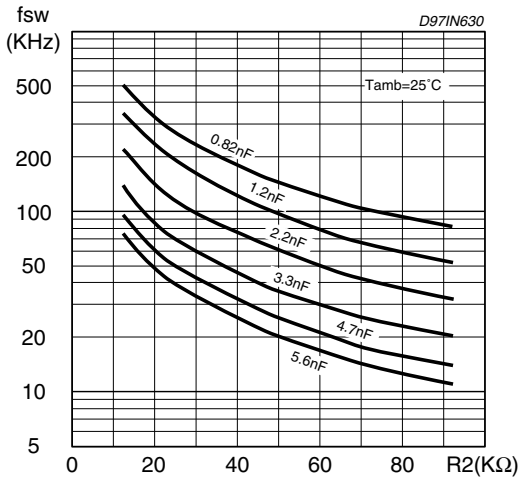
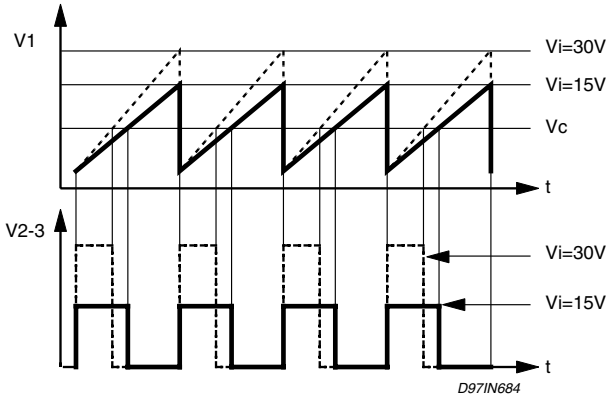


Figure 7. Voltage Feedforward Function.



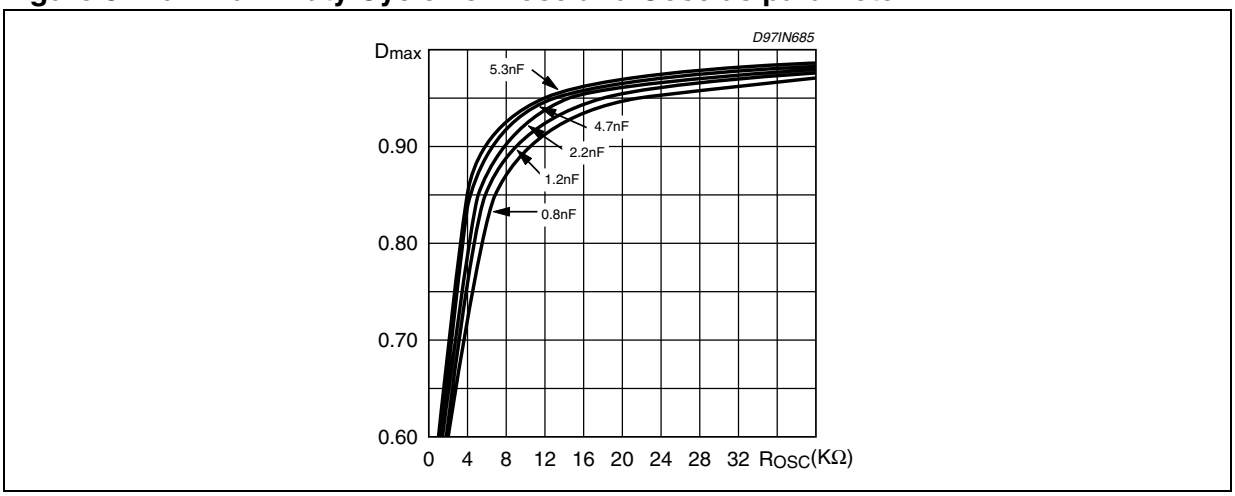
The oscillator peak-to-valley voltage is proportional to the supply voltage, and the voltage feedforward is operative from 8V to 55V of input supply.

$$\Delta V_{osc} = \frac{V_{CC} - 1}{6}$$

Also the $\Delta V/\Delta t$ of the sawtooth is directly proportional to the supply voltage. As Vcc increases, the Ton time of the power transistor decreases in such a way to provide to the chocke, and

finally also the load, the product Volt. sec constant.
Fig 8 show how the ducty cycle varies as a result of the change on the $\Delta V/\Delta t$ of the sawtooth with the Vcc. The output of the error amplifier doesn't change to maintain the output voltage constant and in regulation. With this function on board, the output response time is greately reduced in presence of an abrupt change on the supply voltage, and the output ripple voltage at the mains frequency is greately reduced too.

Figure 8. Maximum Duty Cycle vs. Rosc and Cosc as parameter.



In fact, the slope of the ramp is modulated by the input ripple voltage, generally present in the order of some tents of Volt, for both off-line and dc-dc converters using mains transformers.
The charge and discharge time is approximable to:

$$Tch = R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right)$$

$$Tdis = 100 \cdot C_{osc}$$

The maximum duty cycle is a function of Tch, Tdis and an internal delay and is represented by the equation:

$$Dmax = \frac{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) - 80 \cdot 10^{-9}}{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

and is rapresented in figure 9:

Figure 9. Vo-Io Output Characteristics

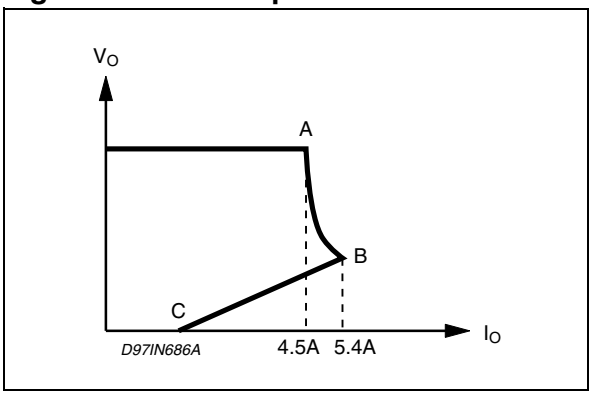
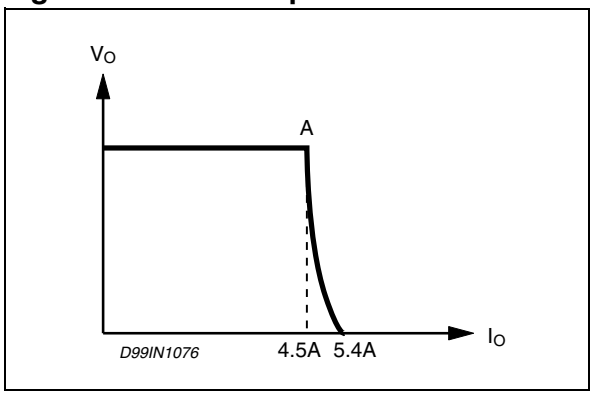


Figure 10. Vo-Io Output Characteristics



3.2 Current protection

The L4973 has two current limit levels, pulse by pulse and hiccup modes.

Increasing the output current till the pulse by pulse limiting current treshold (Ith1 typ. value of 4.5A) the controller reduces the on-time till the value of T_B = 300ns that is a blanking time in which the current limit protection does not trigger. This minimun time is necessary to avoid undesirable intervention of the protection due to the spike current generated during the recovery time of the freewheeling diode.

In this condition, because of this fixed balnking time, the output current is given by:

$$I_{max} = \frac{[V_{CC} \cdot T_B \cdot F_{SW} - V_f \cdot (1 - T_B \cdot F_{SW})]}{[R_O + (R_D + R_L)(1 - T_B \cdot F_{SW}) + (R_{dson} + R_L)T_B \cdot F_{SW}]}$$

Where Ro is the load resistance, Vf is the diode forward voltage. R_D and R_L are the series resistance of, respectively, the freewheeling diode and the choke.

Typical output characteristics are represented in figure 9 and 10 In fig 9, the pulse by pulse protection is sufficient to limit the current.

In fig 10 the pulse by pulse protection is no more effective to limit the current due to the minimun Ton fixed by the blanking time T_B, and the hiccup protection intervenes because the output peak current reachs the relative threshold.

Figure 11. Internal Current Limiting Schematic Diagram.

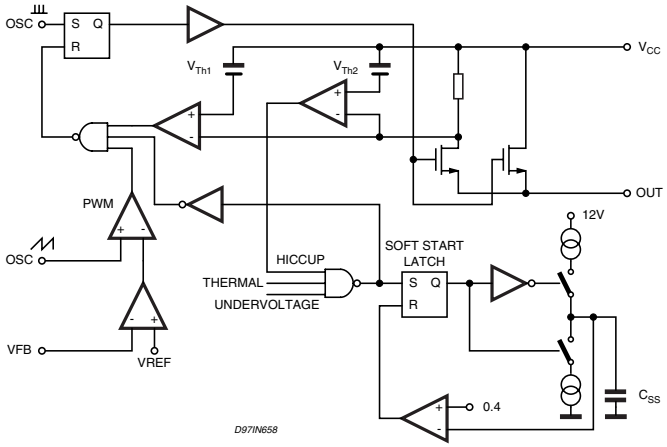
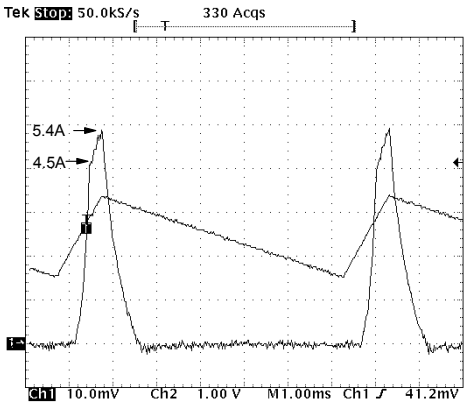


Figure 12. Output current and soft start voltage



At the pulse by pulse intervention (point A) the output voltage drops because of the Ton reduction, and the current is almost constant. Going versus the short circuit condition, the current is only limited by the series resistances R_D and R_L (see relation above) and could reach the hiccup threshold (point B), set 20% higher than the pulse by pulse. Once the hiccup limiting current is operating, in output short circuit condition, the delivered average output current decreases dramatically at very low values (point C).

Fig. 11 shows the internal current limiting circuitry. Vth1 is the pulse by pulse while Vth2 is the hiccup threshold.

The sense resistor is in series with a small mos realized as a partition of the main DMOS.

The Vth2 comparator (20% higher than Vth1) Sets the soft start latch, initializing the discharge of the soft start capacitor at constant current (about 22μA).

When reached about 0.4V, the valley comparator resets the soft start latch, restarting a new soft-start recharging cycle.

Fig. 12 Shows the typicals waveforms of the current in the output inductor and the soft start voltage (pin17).

During the recharging of the soft start capacitor, the Ton increases gradually and, if the short circuit is still present, when Ton>TB and the output peak current reachs the threshold, the hiccup protection intervenes again. So, the value of the soft start capacitor must not be too high (in this case the Ton increases

slowly thus taking much time to reach the TB value) to avoid that during the soft start slope the current exceeds the limit before the protection activation.

The following diagrams of Fig. 13 and Fig. 14 show the maximum allowed soft start capacitor value as a function of the input voltage, inductor value and switching frequency.

A minimun value of the soft start capacitance is necessary to guarantee, in short circuit condition, the functionality of the limiting current circuitry. Infact, with a capacitor too small, the frequency of the current peaks (see figure 11) is high and the mean current value in short circuit increases.

Figure 13. Maximum soft start capacitance with f_{sw} = 100kHz

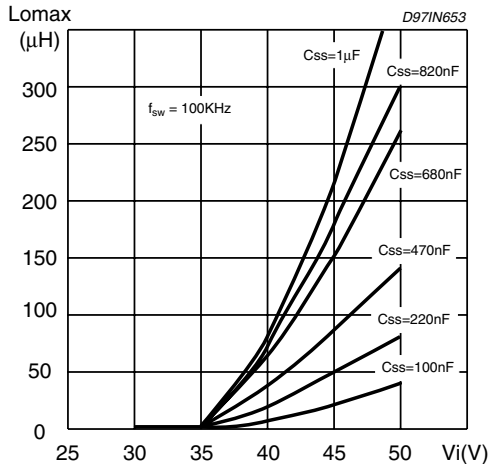
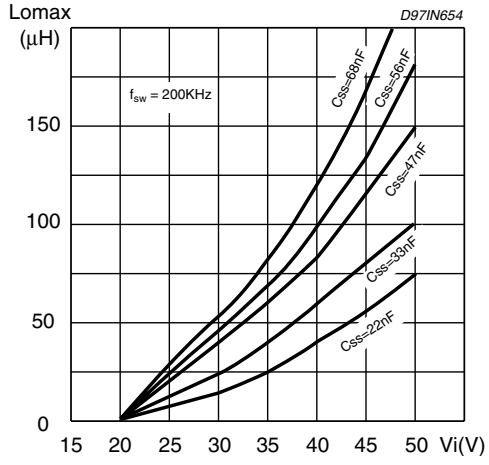
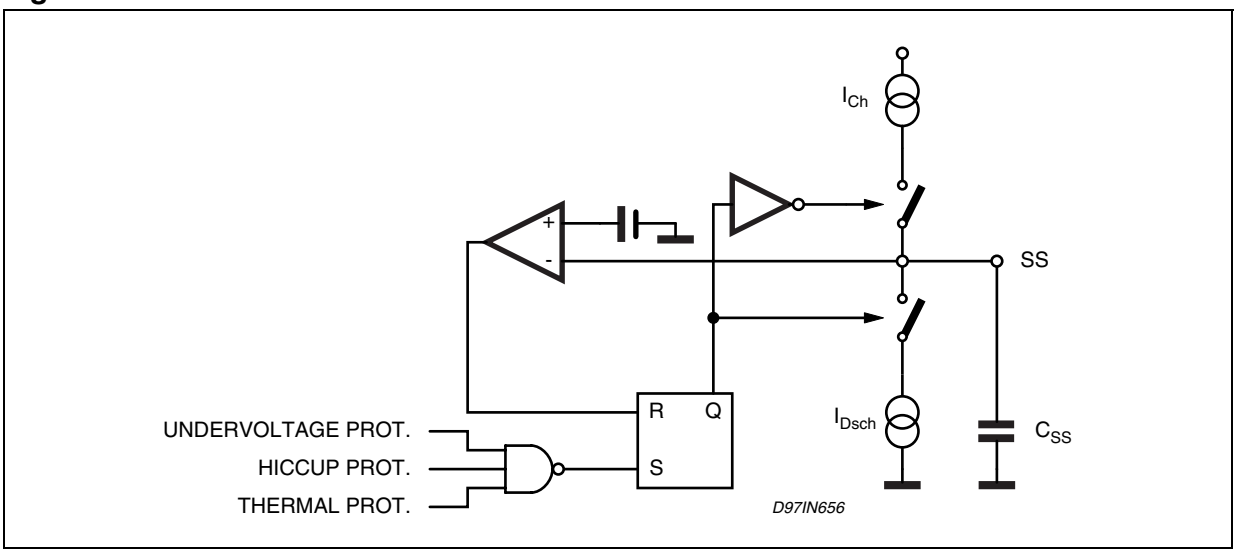


Figure 14. Maximum soft start capacitance with f_{sw} = 200kHz



Example: For a maximum Vcc of 50V, at 100kHz, with an inductor of 140μH, it is possible to use a soft start capacitor lower than 470μF (see fig. 13). With such a value, the soft start time (see fig. 16) of about 10ms for an output voltage of 5V

Figure 15. Soft start internal circuit.



3.3 Soft Start

The soft start function is requested to realize a correct start up of the system without over-stressing the power stage, avoiding the intervention of the current limitating, and having an output voltage rising smoothly without output overshoots.

The Soft start circuit is shown in fig 15. The soft start capacitor is charged at 40 uA, and quickly discharged at power off and in case of thermal shutdown intervention.

The output start-up time is programmable according to the followed formula

$$Tss = \frac{v_o}{i_{CH} \cdot 6 \cdot dMAX} \cdot Css$$

Where Dmax is 0.95.

Soft-start time versus output voltage and Css is shown in Fig. 16.

Thanks to the voltage feedforward the start-up time is not affected by the input voltage.

Fig. 17 shows the output voltage start up using different soft start capacitance values:

Figure 16. Soft start time vs. Vo and Css

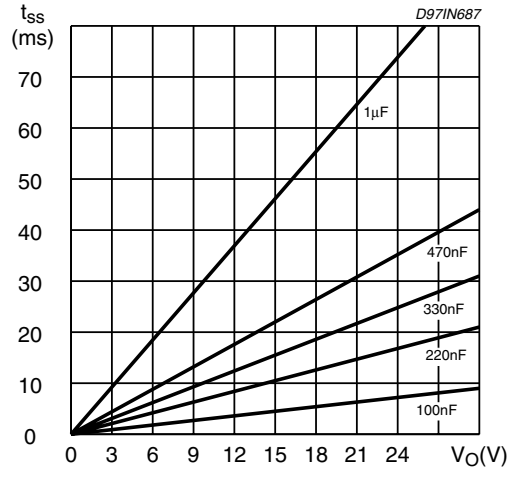
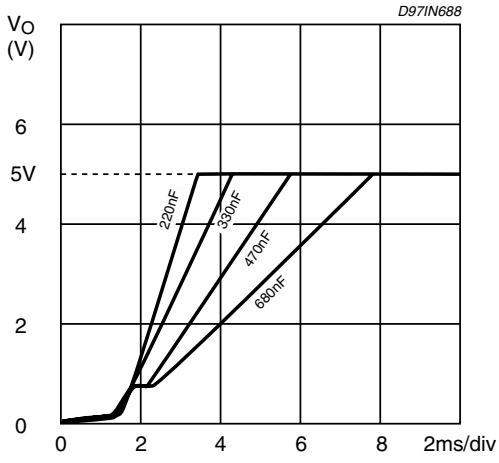


Figure 17. Output rising voltage with Css 680nF, 470nF, 330nF, 220nF.



3.4 Feedback disconnection

In case of feedback disconnection, the duty cycle increases versus the max allowed value bringing the output voltage close to the input supply. This condition could destroy the load. To avoid this dangerous condition, the device is forcing a little current (1.4μA typical) out of the pin 12 (E/A Feedback).
If the feedback is disconnected, open loop, and the impedance at pin 12 is higher than 3.5MΩ, the voltage at this pin goes higher than the internal reference voltage located on the non-inverting error amplifier input, and turns-off the power device.

3.5 Zero load

In normal operation, the output regulation is also guaranteed because the bootstrap capacitor is recharged, cycle by cycle, by means of the energy flowing into the choke. Under light load conditions, this topology tends to operate in burst mode, with random repetition rate of the bursts. An internal new function makes this device capable of keeping the output voltage in full regulation with 1mA of load current only.
Between 1mA and 500μA, the output is kept in regulation up to 8% above the nominal value.
Here the circuitry providing the control :

1) a comparator located on the bootstrap section is sensing the bootstrap voltage; when this is lower than 5V, the internal power VDMOS is forced ON for one cycle and OFF for the next..
2) during this operation mode, i.e. 500μA of load current, the E/A control is lost. To avoid output overvoltages, a comparator with one input connected to pin 12, and the second input connected to a threshold 8% higher that nominal output, turns OFF the internal power device the output is reaching that threshold.
   When the output current, or rather, the current flowing into the choke, is lower than 500μA, that is also the consumption of the bootstrap section, the output voltage starts to increase, approaching the supply voltage.

3.6 Output Overvoltage Protection (OVP)

The output overvoltage protection, OVP, is realized by using an internal comparator , which input is connected to pin 12, the feedback, that turns-off the power stage when the OVP threshold is reached. This threshold is typically 8% higher than the feedback voltage.
When a voltage divider is requested for adjusting the output voltage, the OVP intervention will be setted at:

$$V_{OVP} = 1.08 \cdot V_{fB} \cdot \frac{(Ra + Rb)}{Rb}$$

where Ra is the resistor connected to the output.

3.7 Power Stage

The power stage is realized by a N-channel D-mos transistor with a Vdss in excess of 60V and typ rdson of 150mOhm (measured at the device pins).
Minimising the Rdson, means also minimise the conduction losses.
But also the switching losses have to be taken into consideration. mainly for the two following reasons:

a) they are affecting the system efficiency and the device power dissipation
b) because they generate EMI.

3.8 TURN - ON

At turn-on of the power element, or better, the rise time of the current(di/dt) at turn-on is the most critical parameter to compromise.
At a first approach, it looks that faster is the rise time and lower are the turn-on losses.
It's not completely true.
There is a limit, and it's introduce by the recovery time of the recirculation diode.
Above this limit, about 100A/usec, only disadvantages are obtained:
1- turn-on overcurrent is decreasing efficiency and system reliability
2- big EMI encrease.

Figure 18. Turn on and Turn off (pin 2, 3)

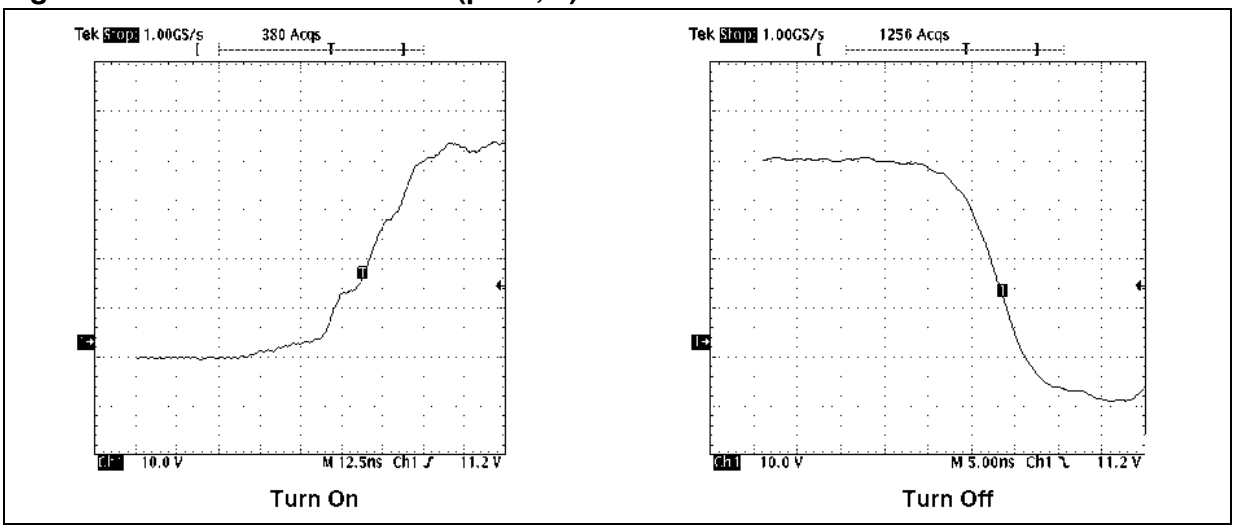
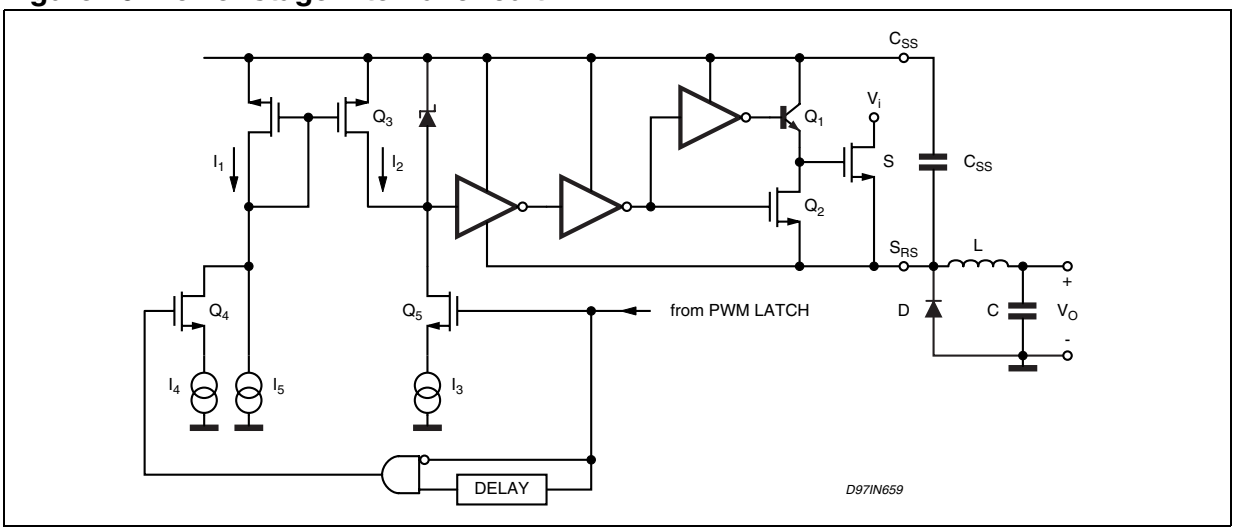


Figure 19. Power stage internal circuit



The L4973 has been developped with a special focus on this dynamic area.
An innovative and proprietary gate driver, with two different timings, has been introduced.
When the diode reverse voltage is reaching about 3V, the gate is sourced with low current (see fig. 18) to assure the complete recovery of the diode without generating unwanted extra peak currents and noise.

After this threshold, the gate drive current is quickly encreased, producing a fast rise time to reach a high efficiency.

Figure 20. Sync and Oscillator waveforms as slave and as master.

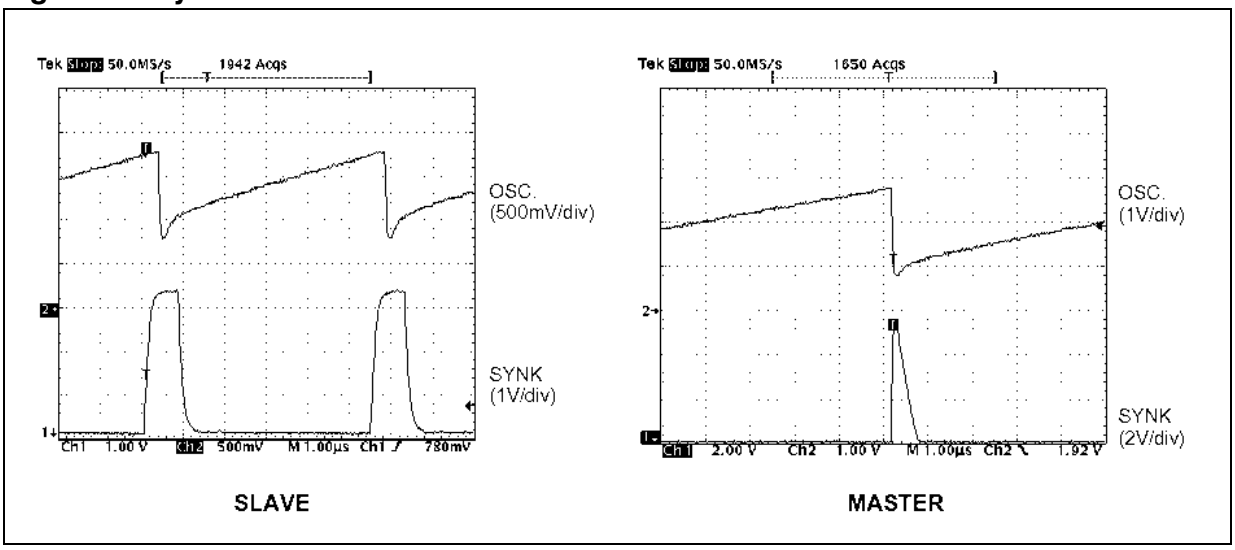
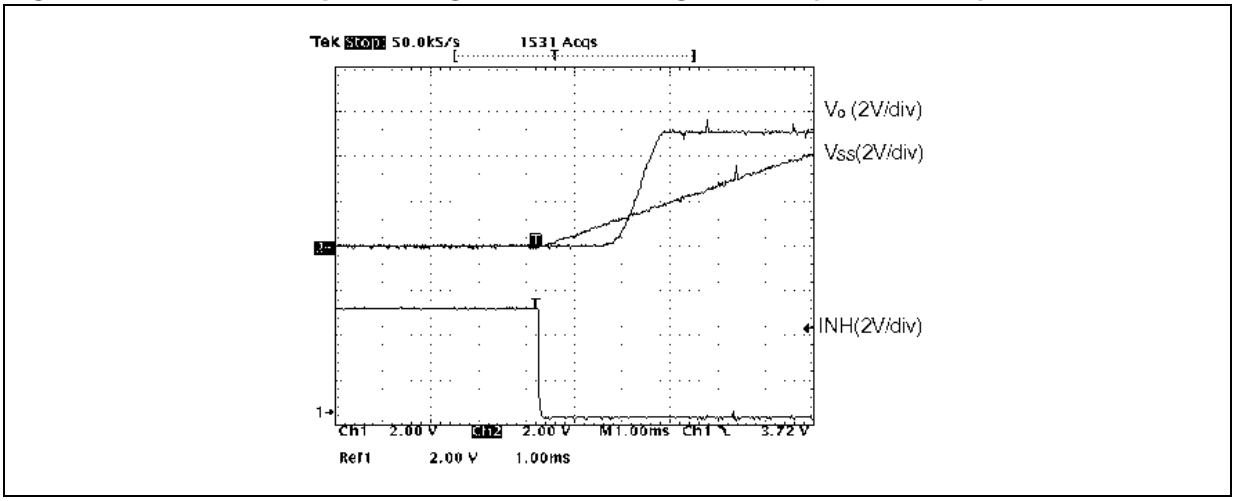


Figure 21. Re-start output voltage when Inhibit goes low (Css = 56nF)



3.9 TURN - OFF

The turn-off behavior, is shown at Fig. 18.

Fig. 19 shows the details of the internal power stage and driver, where at Q2 is demanded the turn-off of the power swicth, S.

3.9.1 Syncronization Function

The device is able to synchronise other L4973s, up to 6.

Moreover, this function has been realized to make the device operating as a master or slave.

As a master, it's able to source a current of 3mA min at 4.5V min. As a slave, it requires a maximum current of 0.45mA and a min pulse width of about 350ns.

Fig. 20 shows the typical syncronization waveforms when the device is used as slave and as master.

3.9.2 Inhibit Function

The Inhibit pin is active high and when left open, is forced to Vcc by an internal current generator and the device is disabled.
In disabled state, Vinh = 5V, the device discharge quickly the soft start capacitor, switch off also the reference voltage, limiting the power consumption to a leakage values only (at 24V, about 100μA) .
Fig. 21 shows the device behavior when inhibit pin goes low; the soft start capacitor is linearly recharged, and the output voltage raises till the nominal value.

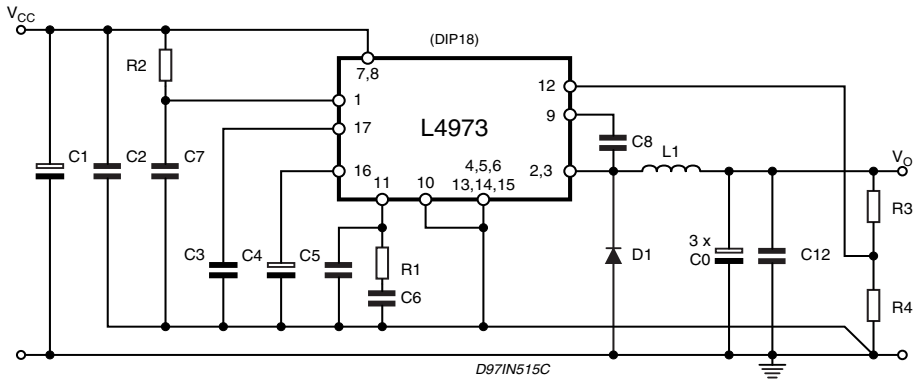
4 TYPICAL APPLICATION.

Fig. 22 shows the typical application circuit, where the input supply voltage, Vcc, can range from 8 to 55V operating, and the output voltage adjustable from 3.3V to 40V.
The selected components, and in particular input and output capacitors, are able to sustain the device voltage ratings, and the corresponding RMS currents.

4.1 Electrical Specification

Input Voltage Range	8V - 55V
Output Voltage	5.1V ±3% (Line, Load and Thermal)
Output Ripple	50mV
Output Current range	1mA - 3.5A
Max Output Ripple current	15% Iomax
Current limit	4.5A
Switching frequency	100kHz
Target Efficiency	85% @ 3.5A Vi = 50V
	95% @ 0.5A Vi = 12V

Figure 22. Application circuit



C1=1000μF/63V
C2=220nF/63V
C3=470nF
C4=1μF/50V
C5=220pF
C6=22nF
C7=2.7nF
C8=220nF/63V
C0=100μF/40V(C9,C10,C11)
C12=Optional (220nF)
L1=150μH $K_{OOL\mu}$ 77310 - 40 Turns - 0.9mm
R1=9.1K
R2=20K
D1=STPS5L60

L4973 V3.3

V_O(V)	R3(KΩ)	R4(KΩ)
3.3	0	
5.1	2.7	4.7
12	12	4.7
15	16	4.7
18	20	4.7
24	30	4.7

L4973 V5.1

V_O(V)	R3(KΩ)	R4(KΩ)
5.1	0	
12	6.2	4.7
15	9.1	4.7
18	12	4.7
24	18	4.7

4.2 Input Capacitor

The input capacitor has to be able to support the max input operating voltage of the device and the max rms input current. The input current is squared and the quality of these capacitors has to be very high to minimise its power dissipation generated by the internal ESR, improving the system reliability. Moreover, input capacitors are also affecting the system efficiency.
The max Irms current flowing through the input capacitors is:

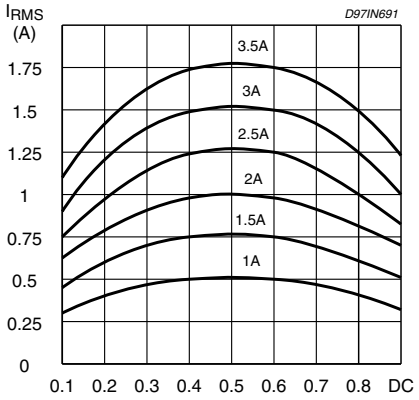
$$I_{rms} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where η is the expected system efficiency, D is the duty cycle and Io the output dc current.
This function reaches the maximum value at D = 0.5 and the equivalent rms current is equal to Io/2. The following diagram Fig. 23 is the graphical rappresentation of the above equation, with an estimated efficiency of 85% , at different output currents.
The maximum and minimum duty cycles are:

$$D_{max} = \frac{V_O + V_f}{V_{ccmin} + V_f} = 0.66 \qquad D_{max} = \frac{V_O + V_f}{V_{ccmax} + V_f} = 0.1$$

where Vf is the freewheeling diode forward voltage. This formula is not taking into account the power mos Rdson, considering negligible the inherent voltage drop, respect input and output voltages. At full load, 3.5A, and D=0.5, the rms capacitor current to be sustained is of 1.75A.
The selected 1000µF/63V EYF or EYS, guaranting a life time of 16000 hours at an ambient temperature of 60°C and switching frequency of 100kHz, can support 1.9A RMS current.

Figure 23. Input Capacitance rms current vs. duty cycle



4.3 Output voltage selection

The two available devices can regulate directly the output voltage respectively the L4973V3.3 the 3.3V and the L4973V5.1, the 5.1V. Each of the two devices can regulate an output voltage higher than the nominal value, up to 40V, by adding an external voltage divider as usually.
In case of requested output voltage lower than 3.3V, it is possible to use the L4973V3.3 with the external connections as shown in fig. 24.

$$V_o = V_{fb} - (V_{ref} - V_{fb}) \cdot \frac{R3}{R5}$$

and the relative function is plotted in fig 25.

Figure 24. Example of output regulated voltage lower than 3.3V

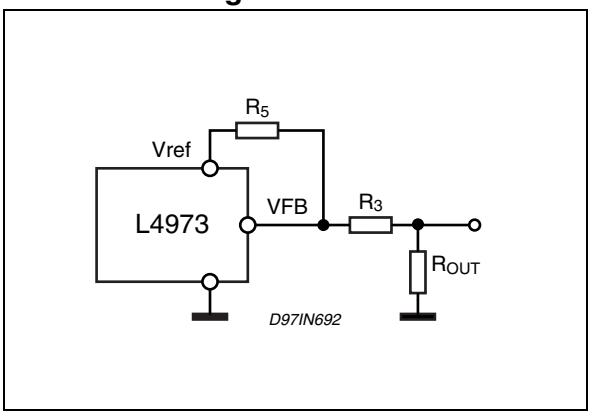
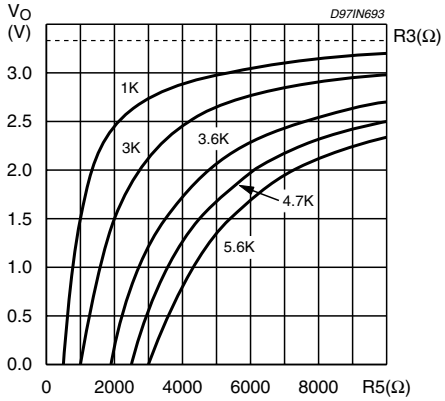


Figure 25. Output voltage vs R5 using R3 as parameter



Only two resistors are used, and all the curves do not intercept the 3.3V but have an asintotic trend to this value.

4.4 Inductor Selection

The criteria used in fixing the inductor value has been dictated by the wanted output ripple voltage, 50mV max., performance obtained of course in combination with output capacitors too. The inductor ripple current, fixed at 10% of Iomax, i.e., 0.35A, requires an inductor value of:

$$L_O = (V_O + V_I) \cdot \frac{(1 - D_{min})}{\Delta I_L \cdot f_{sw}} = 140\mu H \qquad \text{Eq 1}$$

The chocke satisfying this request has to sustain an $L \cdot I^2pk$ of 1.776.
A 77310 (125μ) core, with 40T, can do the job. Material is KoolMμ, from Magnetics.
At full load, the magnetizing force is about 25 Oersted; the inductance value is reduced of about 30% and the ripple current increase at 0.5A (14% of Iomax). It is possible to plot Eq 1 as a function of Vo and Vccmax at 100kHz and 200kHz (see Figg. 26, 27).

Figure 26. Ideal inductor value requested for 10% ripple current, as a function of max. input voltage and output

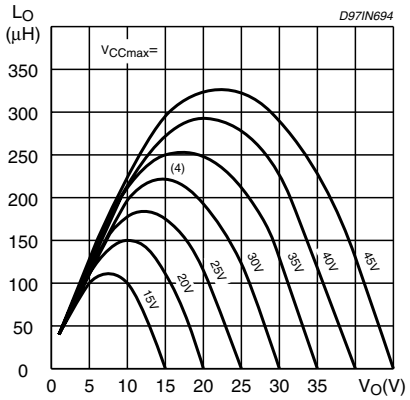
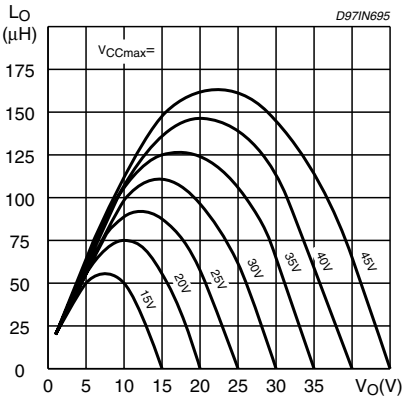


Figure 27. Ideal inductor value requested for 10% ripple current, as a function of max. input voltage and output



Design example: with a maximum input voltage of 30V, at 100kHz, reference curve is number (4) in Fig. 26; with an output voltage of 10V, the suggested inductor value is 200uH.
Core losses are also to be considered when evaluation the system efficiency.
They are proportional to the magnetic flux swing, and to evaluate the magnitude of the flux, the following formula can be used:

$$\Delta B = \frac{L \cdot \Delta I_L \cdot 10^4}{N \cdot A_{le}} = 37mT$$

where N is the number of turns and Ale is the core cross section (cm^2).
The selected core material has the following empirical equation to calculate the core losses:

$$P_l = \Delta B^2 \cdot f_{sw}^{1.5} \cdot V_l \cdot 10^2 = 257mW$$

Where ΔB is in Tesla, f_{sw} in kHz and V_l is the core volume in cm^3. The core increasing temperature is:

$$\Delta T = \left(\frac{P_l}{23.8}\right)^{0.833} = 7.3°C$$

4.5 Output Capacitors

The output capacitors selection, Co, is mainly driven by the output ripple voltage that has to be guaranted, in this case 1% max. of Vo.
The output ripple is defined by the ESR of Co and by the maximum ripple current flowing through it, fixed previously at 0.5A max.
The maximum permitted ESR is:

$$ESR = \frac{\Delta V_O}{\Delta I_L} = \frac{0.051}{0.5} = 102m\Omega$$

The chosed total capacitance is of 3 X 100µF/40V EKR (Frolyt), each of them having an ESR of 230mΩ at 25°C, for a total ripple voltage of 0.76% of Vo, i.e., 40mV.
Co has also to support load transients. An idea of the magnitude of the output voltage drop during load transients is given below:

$$\Delta V_O = \frac{(\Delta I_O)^2 \cdot L_O}{2 \cdot C_O \cdot (V_{inmin} \cdot D_{max} - V_O)} \quad \text{Eq 2}$$

where ΔI_o is the load current change, from 0.5A to 3.5A, Dmax is the max. duty cycle, 95%, Vo nominal is 5.1V, and finally L is 140µH.
Equation 2, normalized at Vo, is represented in the following diagram, Fig. 28, as a function of the minimum input voltage.
These curves are rapresented for different output capacitor 3x100µF, 2x220µF, 3x220µF, 2x470µF all EKR, 40V.

4.6 Compensation Network

The complete controll loop block diagram is shown in fig. 29. The Error Amplifier basic characteristics are:
gm = 2.5mS
Ro = 1.2MΩ

Avo = 60dB
Isource/sink = 300µA

Figure 28. Output drop (%) vs minimum input voltage

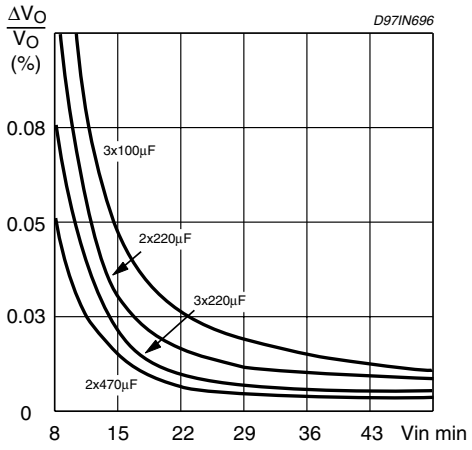


Figure 29. Block diagram compensation loop

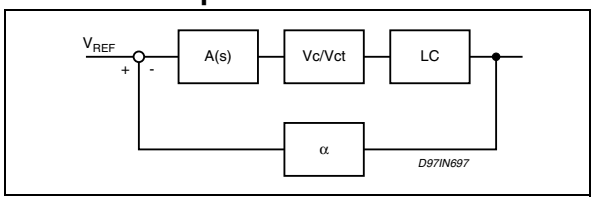


Figure 30.

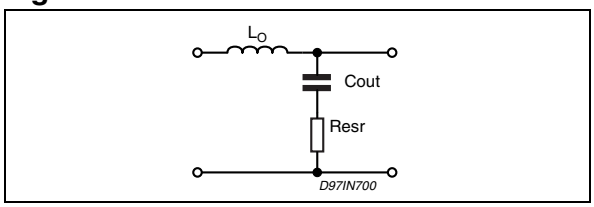
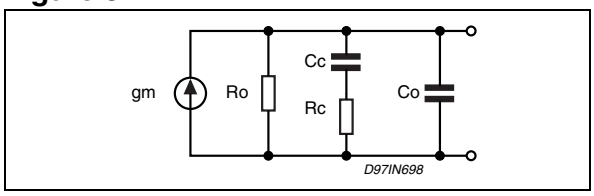


Figure 31.



4.7 Error amplifier and compensation blocks

The open loop gain is:

$$A(s) = gm \cdot \frac{R_O \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot C_o \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot C_o + R_c \cdot C_c) + 1}$$

where Cout is the parallel between the output and the external capacitance of the Error Amplifier and Ro the E/A output impedence. Rc and Cc are the compensation values.

4.8 LC Filter

$$A_{o(s)} = \frac{1 + R_{esr} \cdot C_{out} \cdot s}{L \cdot C_{out} \cdot s^2 + R_{esr} \cdot s + 1}$$

4.9 PWM Gain

$$\frac{V_{CC}}{V_{ct}} = \frac{V_{CC} \cdot 6}{V_{CC} - 1} \approx 6$$

where Vct is the peak to peak sawtooth oscillator.
Poles and zeros value are:

$$F_o = \frac{1}{2 \cdot \pi R_{esr} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot 0.077 \cdot 300 \cdot 10^{-6}} = 6.92KHz$$

$$F_p = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{out}}} = \frac{1}{2 \cdot \pi \cdot \sqrt{140 \cdot 10^{-6} \cdot 300 \cdot 10^{-6}}} = 776Hz$$

$$F_{ocomp} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 9.1 \cdot 10^3 \cdot 22 \cdot 10^{-9}} = 795Hz$$

$$F_{p1} = \frac{1}{2 \cdot \pi \cdot R_o \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 1.2 \cdot 10^{6} \cdot 22 \cdot 10^{-9}} = 6.032Hz$$

$$F_{p2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o} = \frac{1}{2 \cdot \pi \cdot 9.1 \cdot 10^{3} \cdot 220 \cdot 10^{-12}} = 80KHz$$

The compensation is realized choosing the Focomp close to the frequency of the double pole introduced by the LC filter.
Using a compensation network with R1= 9.1K, C6 = 22nF and C5 = 220pF, the Gain and Phase Bode plots are shown in Figg. 32-33. The cut-off frequency and the phase margin are:

Fc = 5KHz Phase margin = 32°

Figure 32. Gain Bode plot open loop

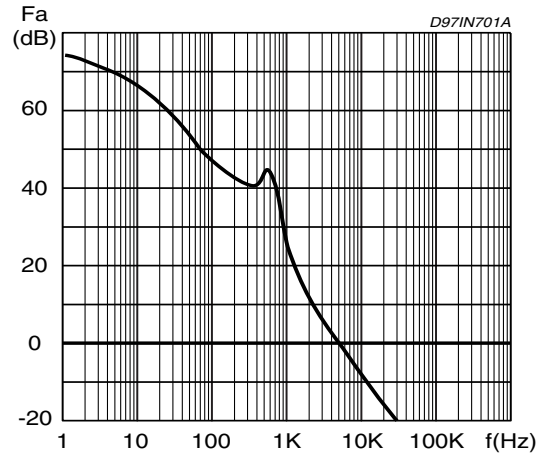
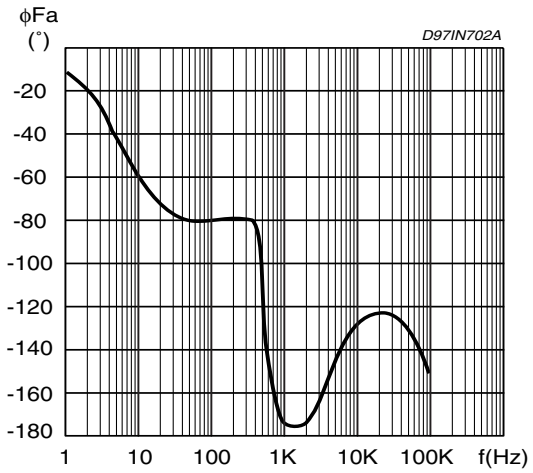


Figure 33. Phase Bode plot open loop

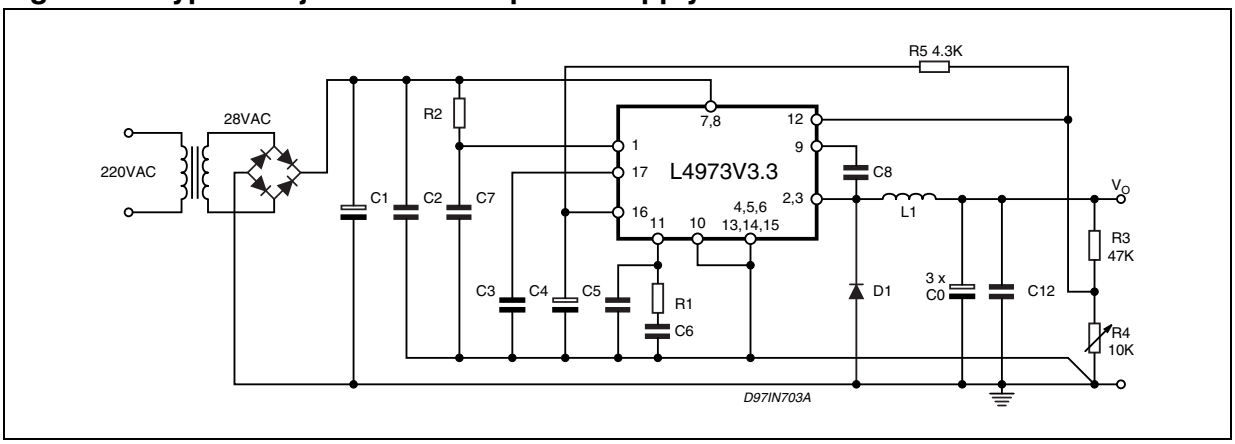


5 APPLICATION IDEAS

5.1 MAINS TRANSFORMER POWER SUPPLY, WITH OUTPUT ADJUSTABLE FROM 0V TO 24V.

Figure 34 shows a power supply including mains transformer, working at 50Hz 220Vac or 60Hz 110Vac, bridge rectifier and filtering capacitor; the output voltage is adjustable from 0 to 24V.

Figure 34. Typical adjustable 0-24V power supply.



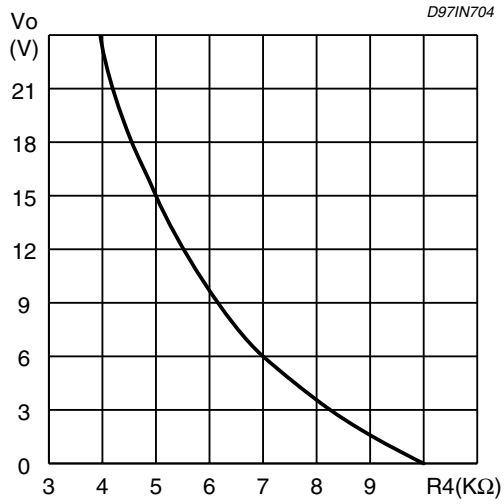
The formula to evaluate the output voltage is:

$$V_o = 3.336 + 3.336 \cdot \left(\frac{R3}{R4} + \frac{R3}{R5}\right) - 5.1 \cdot \frac{R3}{R5}$$

Figure 35 shows the formula plot in which is possible to program the output voltage from 0V to 24V using a 10KΩ potentiomiter as R4. R5 is fixed at 4.3KΩ and R3 is 47KΩ.

Output capacitors have to be chosen with low ESR to reduce the output ripple voltage and load transients.

Figure 35. Output Voltage vs R4



Particular care has to be taken for input filter capacitors because they have to support high ripple current at mains frequency plus the high frequency current.
Total rms current is typically heavy, and very low ESR is requested for system reliability.
Input caps can affect also the system efficiency.
The transformer could be a single secondary winding with four diodes for rectification or centre tapped with two diodes only, but higher reverse voltage.
Considering a max output power close to 100W, equivalent system efficiency of 93-95%, the mains transformer has to be designed around 200VA.
A low voltage secondary pfc can reduce the VA need close to the delivered Watts, 110W, reducing also the electrolitic capacitors value .
Weight and volume of the complete application are also significantly reduced.

5.2 HIGHER INPUT VOLTAGE

Since the max. operating input voltage is 55V, an input line conditioner is requested. Fixing, for example, the device supply voltage at 50V, the power dissipation of the preregulator is :

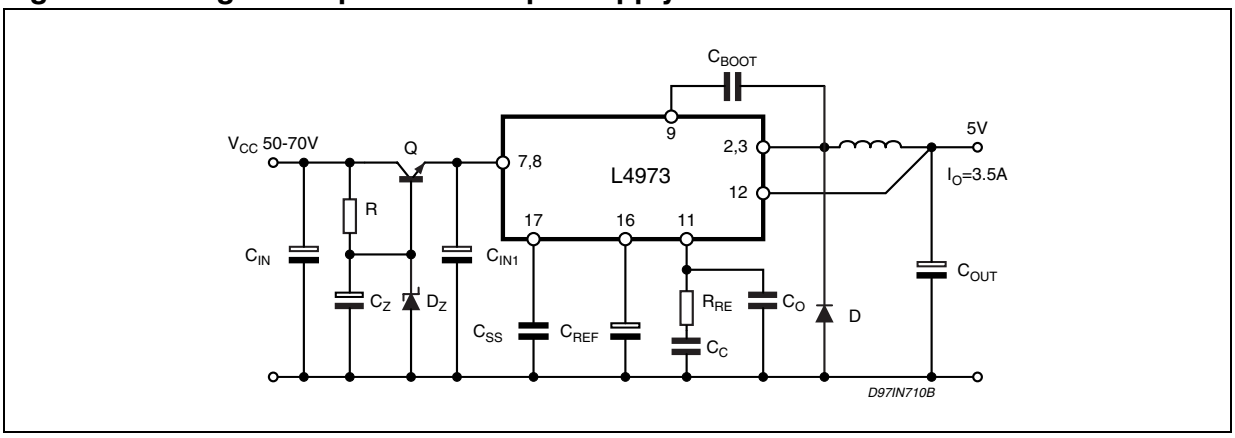
$$Pd = Ii \cdot Vce = Ii \cdot (Vi - 50)$$

In the buck converter, the average input current is:

$$Ii = Io \cdot \frac{Ton}{T} = Io \cdot \frac{Vo}{Vi}$$

- Vo = 5.1V Io = 3.5A Po = 17.85W Ii = 0.357A Pd = 3.57W (Vi = 60V)
- Vo = 12V Io = 3.5A Po = 42W Ii = 0.84A Pd = 8.4W (Vi = 60V)

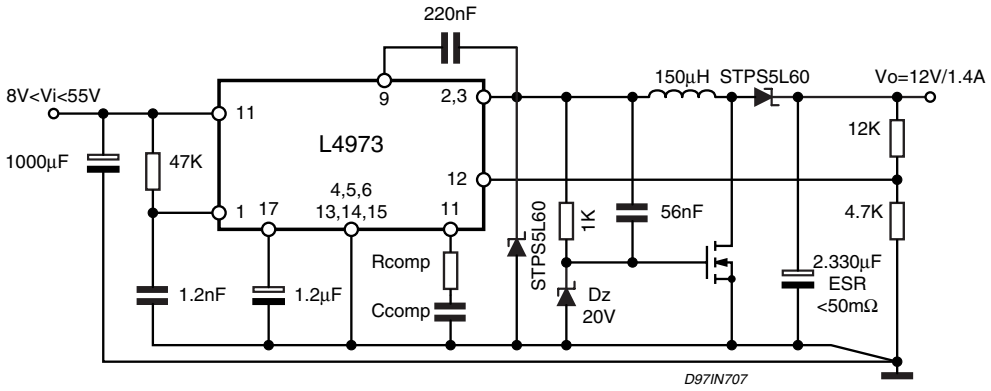
Figure 36. Design example for 70V input supply.



5.3 BUCK-BOOST CONVERTER

This topology is useful to stabilise an output voltage higher, equal or lower than the input supply. Fig 37 shows the schematic diagram of a converter designed for 12V, $I_{out} = 3.5 \times (1\text{-}D)$, with an input supply ranging from 8V to 55V.
The 20V zener connected to gate-source of the power mos is from protection purposes when the supply voltage is higher than 20V.
Such a circuit, asymmetrical half bridge, is fully protected versus output short circuit, by turning-off the on-board floating mos.

Figure 37. Up Down Converter



5.4 CURRENT GENERATOR

Sometime the applications specs requires to generate constant current, fixed or adjustable, for chemical processes, lamp powering, battery chargers for lead acids, ni-cd and ni-me-hyd batteries.

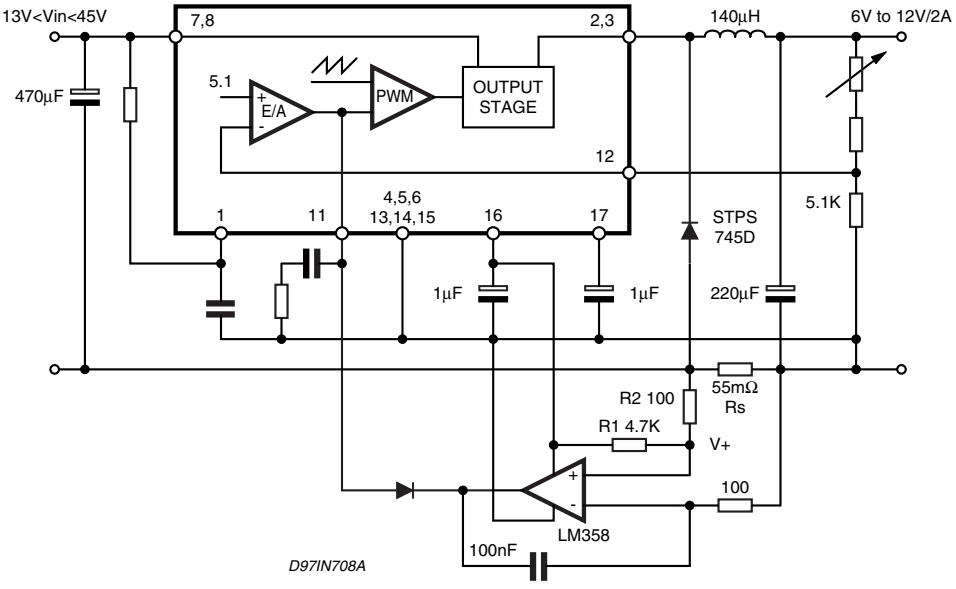
Here, one suggestion will be given for obtaining an accurate constant current generator.

The schematic of Fig 38 propose a simple solution for constant or variable current generator, with good accuracy of the current , using a simple op/amp supplied by the 5.1V available reference voltage.The threshold current is fixed by the voltage divider connected to the n.i. input op/amp, at about 100mV. This is also the max voltage dropping on the current sense resistor Rs. Adjusting the 4.7KOhm, the threshold can be easily changed.

The formula to fix the output current is :

$$I_o = \frac{5.1 \cdot R_2}{(R_1 \cdot R_2) \cdot R_s}$$

Figure 38. Constant current generator, up to 3.5A.



5.5 FROM POSITIVE INPUT TO NEGATIVE OUTPUT

Fig. 39 shows how to obtain a -12V, when only positive supply available.

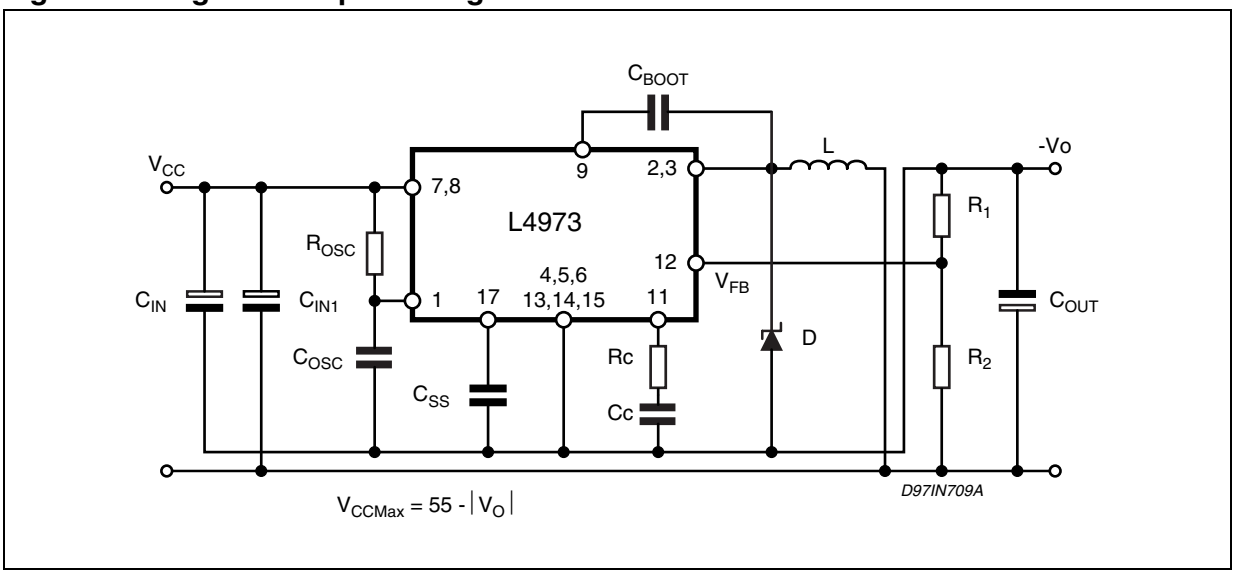
The maximum output current is given by the formula Iout = 3.5 × (1-D) according with the relation for the Buck-Boost topology.

This negative output has to show good precision, stability and regulation, and it must be output short circuit protected.

With the suggested application schematic, one the aim is to satisfy the performance listed above, and to contributing to the simplification of the power transformer, mains or high frequency.

Just to remember not to exceed the absolute maximum voltage rating of the device of 55V operating. In this case the total voltage applied to the device is the addition of the max. positive input voltage with the min. negative output voltage.

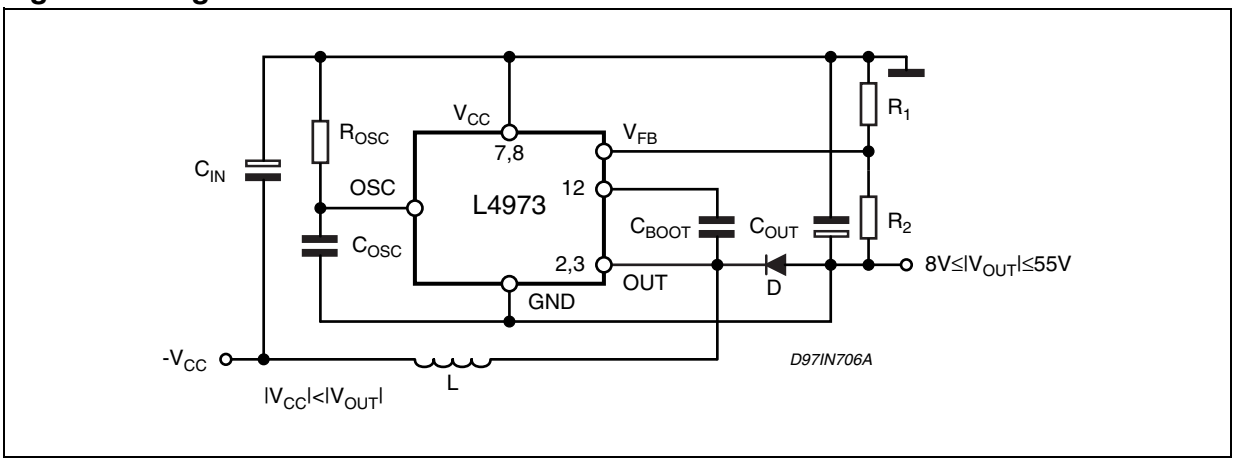
Figure 39. Negative Output Voltage.



5.6 NEGATIVE BOOST CONVERTER

Fig. 40 shows how to stabilise a negative output voltage higher than negative input voltage.

Figure 40. Negative boost converter.



6 REVISION HISTORY

Table 1.

Date	Revision	Description of Changes
October 2000	8	First Issue in EDOCS
May 2005	9	Updated the Layout look & feel. Changed name of the D1 on the fig. 22

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